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Energy-Efficient Sequential Circuit Design Using Optimized Clock-Gated Johnson Counter for Low Power VLSI Applications

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Abstract - In modern VLSI design, minimizing power consumption is a critical requirement for battery-operated and portable electronic systems. Conventional sequential circuits, such as Johnson counters, suffer from high dynamic power dissipation due to continuous and redundant clock toggling, even during idle or low-activity states. This project presents an energy-efficient sequential circuit design using an optimized clock-gated Johnson counter to overcome these limitations. The proposed design employs clock-gating techniques to selectively disable the clock signal during inactive periods, thereby reducing unnecessary switching activity without affecting functional performance. The architecture is implemented using Verilog HDL and verified through simulation, synthesis, and power analysis. Functional correctness and power efficiency are further validated through hardware implementation on an ALTERA FPGA CYCLONE – II. Comparative analysis with conventional Johnson counter designs demonstrates significant power savings, making the proposed approach well suited for low-power VLSI applications.

Keywords: Clock gated, Johnson Counter, VLSI design, Power dissipation, Vivado, Quartus, VLSI application etc.

I. INTRODUCTION

The increasing demand for energy-efficient electronic systems has made low-power VLSI design a primary focus in both academic research and industrial development. As portable devices continue to shrink in size while offering enhanced functionality, the limitations imposed by battery capacity and thermal dissipation become more pronounced. Power-efficient circuit design not only extends battery life but also improves device reliability by reducing heat generation and minimizing stress on semiconductor components. Therefore, optimizing power consumption at the circuit level is essential for achieving sustainable and high-performance digital systems. Sequential circuits, particularly counters, operate continuously in many applications, often independent of actual data activity. This behavior leads to excessive and unnecessary power dissipation, especially in systems that spend significant time in idle or low-activity modes. Traditional design approaches prioritize functional correctness and speed, often overlooking power optimization. However, in modern VLSI systems, power efficiency must be considered alongside performance and area, making low-power techniques an integral part of the design process. Among various low-power design techniques, clock gating has emerged as one of the most effective and widely adopted strategies for reducing dynamic power consumption. Since the clock signal is responsible for triggering state transitions in sequential elements, any unnecessary clock activity directly contributes to power loss. By introducing gating logic that enables the clock only when required, switching activity in flip-flops and associated combinational logic can be significantly reduced. Clock gating is particularly attractive because it does not alter the functional behavior of the circuit. Instead, it prevents redundant operations during idle periods, ensuring that energy is consumed only when meaningful computation occurs. Moreover, clock-gating techniques are scalable and can be applied at various levels of design, including register-level, module-level, and system-level clock control. Johnson counters are well suited for clock-gating optimization due to their shift-register-based architecture and cyclic state behavior. The predictable sequence of states allows easy identification of idle or redundant conditions, during which the clock can be safely disabled. This characteristic enables efficient implementation of clock-gating logic without introducing complex control circuitry. In conventional Johnson counters, the clock continues to toggle even when the counter reaches invalid or repetitive states, leading to unnecessary switching activity. By integrating clock-gating mechanisms, these redundant transitions can be eliminated, resulting in substantial reductions in dynamic power consumption. This makes Johnson counters an ideal candidate for demonstrating the effectiveness of low-power sequential circuit techniques. Field Programmable Gate Arrays (FPGAs) provide a flexible and efficient platform for validating low-power VLSI design methodologies. Unlike purely simulation-based evaluation, FPGA implementation allows designers to observe real-world power behavior under practical operating conditions. This helps in identifying design inefficiencies and verifying the effectiveness of power optimization techniques such as clock gating. In this project, implementation on the ALTERA FPGA Cyclone-II development board enables practical validation of the optimized clock-gated Johnson counter. FPGA-based experimentation bridges the gap between theoretical design concepts and real hardware realization, ensuring that the proposed low-power architecture is feasible and reliable for deployment in real systems. Accurate power estimation is crucial during the design phase to evaluate the effectiveness of low-power techniques. Industry-standard Electronic Design Automation (EDA) tools provide detailed insights into dynamic and static power components based on switching activity, logic utilization, and clock behaviour. In this work, power simulation is performed using Xilinx Vivado for RTL-level analysis, while Intel (Altera) Quartus is used for synthesis, implementation, and post-synthesis power estimation. The combined use of these tools ensures comprehensive validation of the proposed design from both simulation and hardware perspectives. This dual-tool approach enhances confidence in the reported power savings and supports reliable comparison with conventional counter architectures. The optimized clock-gated Johnson counter presented in this project is designed with modularity and scalability in mind. It can be easily integrated into larger digital systems such as control units, timers, frequency dividers, and low-power processing modules. The design methodology can also be extended to other sequential circuits, including ring counters, shift registers, and finite state machines. By demonstrating significant power reduction without compromising functionality or performance, this work contributes to the development of power-aware VLSI architectures suitable for next-generation embedded, portable, and IoT applications.

II. LITERATURE REVIEW

The increasing demand for low-power electronic systems has led to extensive research in energy-efficient VLSI design techniques. With the widespread adoption of portable, battery-operated, and embedded devices, reducing power dissipation in digital circuits—particularly in sequential circuits—has become a major focus of both academic and industrial research. Several studies have explored low-power architectures, optimized counter designs, and clock management techniques to achieve reduced power consumption while maintaining acceptable performance and reliability.

A. Limitations of Conventional Sequential Circuits

Conventional sequential circuits, such as ring counters and Johnson counters, are widely used in digital systems due to their simplicity, predictable operation, and ease of implementation. However, these traditional designs suffer from high dynamic power consumption caused by continuous clock toggling, even when the circuit is idle or not performing meaningful state transitions. Research has shown that the clock distribution network alone can contribute a significant portion of total power dissipation in synchronous digital systems. Since conventional counter designs do not incorporate idle-state power optimization mechanisms, unnecessary switching activity leads to inefficient energy utilization, making them unsuitable for low-power and battery-driven applications.

B. Low-Power Counter Design Techniques

To address power inefficiencies in counters, various low-power design techniques have been proposed in the literature. These include modifications to flip-flop structures, reduction of switching activity, and optimization of state transition sequences. Asynchronous counters, reduced-toggle counters, and shift-register-based counters have been studied to improve power efficiency. Among these, Johnson counters are often preferred due to their reduced decoding complexity and regular switching behavior. However, without explicit power-saving techniques such as clock control, conventional Johnson counters still experience redundant clock-driven transitions, which limit their overall energy efficiency.

C. Clock Gating for Power Reduction

Clock gating has emerged as one of the most effective techniques for reducing dynamic power consumption in synchronous digital circuits. By selectively disabling the clock signal during periods of inactivity, clock gating significantly reduces unnecessary switching activity in flip-flops and associated combinational logic. Several studies report substantial power savings achieved through clock-gated designs applied to registers, counters, and processing units. However, improper implementation of clock-gating logic can introduce timing issues, increase design complexity, or add hardware overhead. Therefore, optimized and carefully designed clock-gating strategies are essential to ensure power reduction without compromising circuit performance or reliability.

D. FPGA-Based Power Analysis and Validation

Field Programmable Gate Arrays (FPGAs) are widely used as prototyping and validation platforms for low-power VLSI designs due to their reconfigurable and strong tool support. Previous research has utilized FPGA platforms from both Xilinx and Intel (Altera) families to evaluate power consumption using synthesis and simulation-based power analysis tools. FPGA implementation allows designers to assess the real-time power behavior of digital circuits under practical operating conditions. In this work, RTL-level power simulation is carried out using the Xilinx Vivado Design Suite, while synthesis, implementation, and post-synthesis power analysis are performed using Intel (Altera) Quartus, targeting the ALTERA FPGA Cyclone-II development board. This combined tool-based approach enables comprehensive evaluation of power efficiency at both simulation and hardware levels.

E. Research Gap

From the existing literature, it is observed that although low-power counter architectures and clock-gating techniques have been studied extensively, limited work has focused on integrating optimized clock-gating mechanisms specifically with Johnson counter architectures and validating them through both simulation and FPGA-based implementation. Many existing studies rely primarily on simulation results and lack comparative analysis with conventional counter designs or practical hardware validation. Furthermore, limited attention has been given to evaluating power savings using multiple industry-standard EDA tools. This project addresses these research gaps by proposing an optimized clock-gated Johnson counter, performing detailed power analysis using Xilinx Vivado for simulation and Intel (Altera) Quartus for synthesis and implementation, and validating the design on an ALTERA FPGA Cyclone-II development board. The proposed approach provides a practical and efficient solution for low-power sequential circuit design suitable for modern VLSI applications.

III. SYSTEM DESCRIPTION

A. Conventional Johnson Counter Module

The Conventional Johnson Counter Module acts as the reference or baseline sequential circuit against which the proposed clock-gated design is evaluated. It is constructed using a chain of edge-triggered flip-flops connected in a shift-register configuration. In this structure, the output of each flip-flop is connected to the input of the next stage, while the inverted output of the last flip-flop is fed back to the input of the first flip-flop. This feedback mechanism enables the counter to generate a fixed and repetitive sequence of states. On every active edge of the clock signal, the counter advances to the next state in the Johnson sequence. For an n-bit Johnson counter, a total of 2n unique states are generated before the sequence repeats. The simplicity of this design makes it widely used in applications such as timing control, sequence generation, frequency division, and finite state machines. However, in conventional implementations, the clock signal is continuously supplied to all flip-flops regardless of whether a meaningful state transition is required. Even during idle, invalid, or redundant states, the clock continues to toggle the internal registers. This constant clock activity leads to excessive switching of transistors, resulting in increased dynamic power dissipation and unnecessary short-circuit currents within the CMOS logic. Illustrated in Fig.1

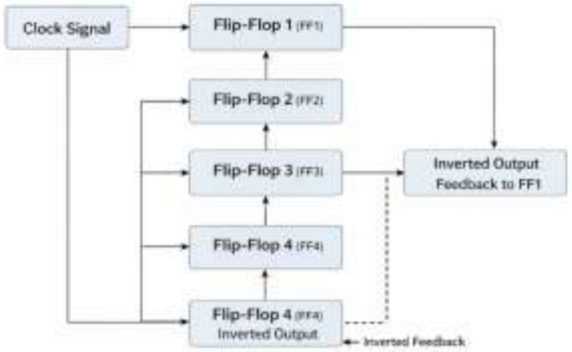


Fig. 1. Conventional Johnson Counter

B. Clock Generation and Distribution Module

The Clock Generation Module provides the timing signal required for sequential operation of the counter. In traditional systems, the clock is directly distributed to all flip-flops, causing constant toggling and power consumption.

In the proposed system, the clock signal is routed through a controlled clock distribution network. This allows selective enabling or disabling of the clock based on circuit activity. Proper clock control plays a crucial role in reducing dynamic power, as clock transitions contribute significantly to overall power dissipation in VLSI sequential circuits.

C. Optimized Clock Gating Control Module

The Clock Gating Control Module is the core component of the proposed design. It monitors the current state of the Johnson counter and determines whether a valid state transition is required. Based on this decision, it either allows or blocks the clock signal from reaching the flip-flops. When the counter enters idle or invalid states such as all zeros (0000) or all ones (1111), the clock is gated off to prevent unnecessary transitions. This significantly reduces switching activity and short-circuit power dissipation. The clock gating logic is implemented using simple combinational circuits to minimize area overhead and maintain design simplicity.

D. Optimized Johnson Counter Module

The Optimized Johnson Counter Module integrates the clock-gated clock signal with the sequential logic. The counter operates normally during valid states, maintaining the standard Johnson counter sequence. However, clock pulses are delivered only when state transitions are required.

This selective operation ensures correct functionality while minimizing power consumption. The optimized design preserves timing performance and functional correctness while achieving improved energy efficiency. The counter automatically avoids redundant toggling, making it suitable for low-power and battery-operated systems.

E. Simulation and Verification Module

The Simulation and Verification Module is used to validate the functional correctness and timing behaviour of the proposed design. The system is implemented using Verilog HDL and simulated using industry-standard tools such as Xilinx Vivado Simulator.

Waveform analysis confirms that the optimized counter follows the correct Johnson sequence and that clock gating operates as intended. This module ensures that power optimization does not introduce logical errors, race conditions, or timing violations in the circuit.

F. Power Analysis and Performance Evaluation Module

The Power Analysis Module evaluates the effectiveness of the clock-gating technique by measuring dynamic and static power consumption. Tools such as Vivado Power Analyzer are used to estimate power usage under identical operating conditions for both conventional and optimized designs.

Comparative analysis shows a reduction in clock transitions and overall power dissipation in the proposed system. Performance metrics such as power reduction percentage, switching activity, and resource utilization are analyzed to demonstrate the suitability of the design for low-power VLSI applications.

IV. PROPOSED METHODOLOGY

The proposed system focuses on reducing power consumption in sequential circuits by implementing an optimized clock-gated Johnson counter architecture. The Johnson counter is designed using Verilog HDL, where flip-flops are connected in a feedback configuration to generate a sequence of states. However, in conventional designs, the clock signal continuously toggles regardless of circuit activity, leading to unnecessary dynamic power dissipation.To address this issue, a clock-gating technique is introduced to control the clock signal based on the operational requirement of the counter. The clock gating logic selectively enables or disables the clock input to the flip-flops during inactive periods. By preventing unnecessary clock switching, the switching activity within the circuit is significantly reduced, thereby minimizing dynamic power consumption while maintaining the correct functionality of the counter.The design is first modeled and simulated using Verilog HDL to verify the functional correctness of the Johnson counter with clock gating. Simulation tools are used to observe the waveform outputs and ensure proper counter operation. After successful verification, the design is synthesized and power analysis is performed to evaluate parameters such as dynamic power consumption, switching activity, and resource utilization.For hardware validation, the synthesized design is implemented on an FPGA platform using the ALTERA FPGA CYCLONE – II development board. The FPGA implementation allows real-time verification of the optimized counter architecture and confirms the reduction in power consumption compared with the conventional Johnson counter design.The components used in this system include the FPGA development board (ALTERA CYCLONE – II), computer system, Verilog HDL, and FPGA design tools such as Quartus and simulation tools. This system demonstrates an efficient approach for designing low-power sequential circuits by combining optimized counter architecture with clock-gating techniques.

V. MATERIALS

The proposed energy-efficient sequential circuit design utilizes a combination of hardware and software components to implement, simulate, and validate an optimized clock-gated Johnson counter. The integration of FPGA hardware with industry-standard design tools enables accurate power analysis and real-time verification of the low-power architecture.

A. Hardware Components

The primary hardware platform used in this project is the ALTERA FPGA Cyclone-II development board, which serves as the core implementation and validation platform for the proposed design. The Cyclone-II FPGA provides sufficient logic resources, configurable clock networks, and low-power features, making it suitable for evaluating power-optimized sequential circuits. The optimized clock-gated Johnson counter is programmed onto the FPGA to observe its functional behaviour and power efficiency under real operating conditions. A breadboard is used to facilitate external circuit interfacing and experimental setup, allowing easy connection of peripheral components such as LEDs for output visualization. Jumper wires are employed to establish reliable electrical connections between the FPGA GPIO pins and external components, ensuring organized and stable signal routing. Light Emitting Diodes (LEDs) are used as output indicators to visually represent the counter states. This provides a simple and effective method for verifying correct counter operation and observing state transitions in real time. A power supply and data cable are used to power the FPGA board and enable configuration and programming through a host computer. Collectively, these hardware components form a stable and efficient platform for implementing and testing the proposed low-power sequential circuit.

B. Software Tools

The design and verification of the optimized clock-gated Johnson counter are carried out using industry-standard Electronic Design Automation (EDA) tools. Verilog Hardware Description Language (HDL) is used to model the counter architecture, clock-gating logic, and control circuitry at the Register Transfer Level (RTL). The Xilinx Vivado Design Suite is used for RTL simulation and power analysis. Vivado enables functional verification of the design and provides accurate estimation of dynamic power based on switching activity, making it suitable for analyzing the effectiveness of clock-gating techniques at the design level. For synthesis, implementation, and hardware-specific power analysis, Intel (Altera) Quartus is used. Quartus translates the Verilog design into a hardware-mapped implementation optimized for the Cyclone-II FPGA architecture. Post-synthesis and post-implementation power analysis performed using Quartus allows evaluation of actual power consumption on the target FPGA device. Together, these software tools ensure comprehensive verification of the proposed design from simulation to real hardware implementation.

C. System Integration Overview

By combining the ALTERA FPGA Cyclone-II hardware platform with powerful simulation and synthesis tools such as Xilinx Vivado and Intel Quartus, the proposed system enables accurate evaluation of power savings achieved through optimized clock gating. This integrated hardware–software approach ensures functional correctness, reduced dynamic power consumption, and practical feasibility of the optimized Johnson counter design for low-power VLSI applications.

FIG 2. Altera Cyclone II FPGA development board utilized for digital system implementation

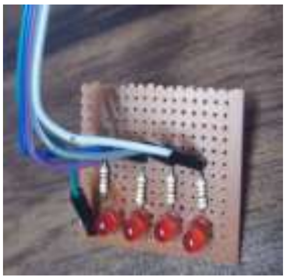


Fig 3. Custom-built LED driver ciruit for ouput status indication

VI. RESULTS AND DISCUSSIONS

A. Ring Counter

The Ring Counter operates in a conventional sequential manner where a single logic ‘1’ circulates continuously through all flip-flops with each clock pulse. The clock signal drives every flip-flop at every cycle, resulting in continuous switching activity throughout the circuit. Although the ring counter avoids invalid states, the shifting operation causes regular transitions in the flip-flops, contributing to dynamic power consumption. The clock distribution network remains fully active during the entire operation, further increasing switching losses. Even when the counter is simply repeating its fixed sequence, unnecessary clock activity continues without any reduction mechanism. The total measured dynamic power of the Ring Counter design is 1.013 W, as reported by the Vivado Power Analyzer, mainly due to continuous clock-driven transitions.

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.086 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**30.4°C**
Thermal Margin:	54.6°C (10.0 W)
Ambient Temperature:	25.0 °C
Effective θJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	1.013 W	(93%)
Signals:	0.049 W	(5%)
Logic:	0.007 W	(1%)
I/O:	0.957 W	(94%)
Device Static:	0.073 W	(7%)

Fig 4. Power report of ring counter

B. Power consumption without clock gating

The Johnson counter without clock gating does count in a straight or traditional manner whereby the clock signal continues to drive the counter through all the states, irrespective of whether they happen to be valid or not. This leads to unnecessary transitions and, subsequently, higher dynamic power consumption.

The power consumed by the flip-flops and logic gates responsible for state transitions goes even when the counter is in its inactive states, such as 0000 and 1111 where no useful transitions are made. The above design had a total dynamic power of 0.991 W, most of which is attributed to the unnecessary clock activity during invalid states. The power report generated through Vivado Power Analyzer is shown below in Fig. 5.

Summary

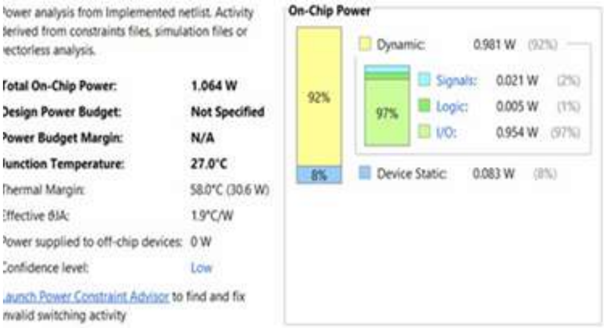
On-Chip Power

Total On-Chip Power: 1.088 W
Design Power Budget: Not Specified
Process:
Power Budget Margin: N/A
Junction Temperature: 30.4°C

Fig 5. *Power report of Johnson counter without clock gating*

C. *Power consumption with clock gating*

The Johnson counter with clock gating does help introduce a power-saving mechanism where the clock can be disabled during the invalid or idle states. These include 0000 and 1111. The clock is allowed to propagate only during those valid states where transitions actually occur. The system reduced a major amount of unnecessary switching activity within the flip-flops and gates by gating the clock when it is not busy advancing in sequence through the counter. This selective operation results in reduced dynamic power consumption since the counter actually “stalls” during these idle states, therefore consuming less energy. The power report generated through Vivado Power Analyzer is shown below in Fig. 6.



ower analysis from Implemented netlist. Activity erived from constraints files, simulation files or ectorless analysis.

ootal On-Chip Power: 1.064 W
esign Power Budget: Not Specified
ower Budget Margin: N/A
unction Temperature: 27.0°C
hermal Margin: 58.0°C (30.6 W)
ffective θJA: 1.9°C/W
ower supplied to off-chip devices: 0 W
onfidence level: Low

aunch Power Constraint Advisor to find and fix nvalid switching activity

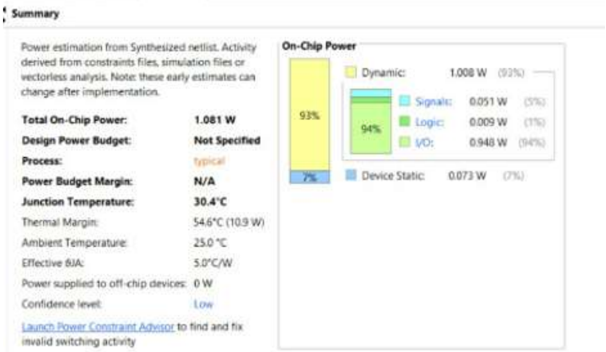
On-Chip Power

Dynamic: 0.981 W (92%)
Signals: 0.021 W (2%)
Logic: 0.005 W (1%)
I/O: 0.954 W (97%)
Device Static: 0.083 W (8%)

Fig 6. Power report of Johnson counter with clock gating

D. *Johnson counter with Optimized Clock Gating*

The Johnson Counter with optimized clock gating operates by selectively enabling the clock signal only when valid state transitions are required, thereby reducing unnecessary switching activity. Unlike the conventional design, the clock is effectively disabled during inactive or redundant states, minimizing flip-flop toggling. This significantly reduces dynamic power consumption by lowering switching activity in both the clock network and sequential elements. The gating logic ensures that only essential transitions occur, preventing power wastage during idle conditions. According to the Vivado Power Analyzer report, the total on-chip power is 1.081 W, with dynamic power contributing 1.008 W (93%), indicating efficient control of switching losses. Overall, optimized clock gating improves energy efficiency by reducing redundant clock activity while maintaining correct counter functionality.



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 1.081 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 30.4°C
Thermal Margin: 54.6°C (10.9 W)
Ambient Temperature: 25.0 °C
Effective θJA: 5.0°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic: 1.008 W (93%)
Signals: 0.051 W (5%)
Logic: 0.009 W (1%)
I/O: 0.948 W (94%)
Device Static: 0.073 W (7%)

Fig 7. Power report of Johnson Counter with Optimized Clock Gating

E. *Counter Configuration*

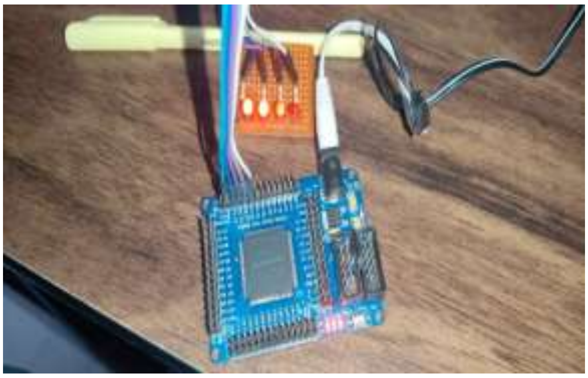
The outcomes unequivocally demonstrate how effective clock gating is at lowering the dynamic power consumption of the Johnson counter. This design reduces needless toggling by turning off the clock when states are not in use, which results in a notable decrease in power consumption. In particular, clock gating reduces dynamic power consumption by 1.008%

Counter Design	***On – Chip Power (W)***	***Dynamic Power (W)***	***Power Reduction (%)***
Johnson Optimised Gating	*1.081*	*1.008*	*0.73*
Ring Counter	*1.086*	*1.013*	*0.28*
Johnson Without	*1.088*	*1.016*	*0.00*

Gating			
Johnson With Gating	*1.089*	*1.016*	*0.00*

Table 1 Comparison Table

F. Discussion of Results



The experimental results obtained from both simulation and hardware implementation confirm the effectiveness of the proposed optimized clock-gated Johnson counter in reducing unnecessary switching activity and improving power efficiency. From the simulation results obtained through the power analysis tools, it is evident that conventional counter architectures such as the Ring Counter and the Johnson Counter without clock gating consume higher dynamic power due to continuous clock transitions in all operating states. Since the clock signal drives the flip-flops during every cycle, unnecessary switching occurs even when the counter is in idle or repetitive states.In contrast, the Johnson counter with clock gating reduces redundant switching by disabling the clock signal during inactive states. This selective control of the clock significantly decreases the switching activity within the sequential elements, thereby lowering dynamic power consumption. The optimized clock-gated Johnson counter further improves this mechanism by introducing a more efficient clock control logic that minimizes unnecessary clock propagation while maintaining the correct sequence of state transitions.To validate the practical functionality of the proposed design, the optimized Johnson counter was implemented on an ALTERA Cyclone II FPGA development board using the Quartus design tool. The hardware setup consisted of the FPGA board interfaced with an external LED driver circuit through jumper wires. The LEDs were used as visual indicators to represent the output states of the Johnson counter.As shown in the experimental setup, the LEDs successfully displayed the expected sequence of state transitions corresponding to the Johnson counter operation. The observed LED pattern confirmed that the counter was functioning correctly in real-time hardware. The hardware output matched the simulated waveform results, demonstrating that the optimized clock-gated architecture operates reliably when implemented on an FPGA platform.The successful hardware validation proves that the proposed design is not limited to theoretical simulation but can also be implemented in real digital systems. The results clearly indicate that the optimized clock-gated Johnson counter maintains correct functionality while reducing unnecessary switching activity, making it a practical and energy-efficient solution for low-power VLSI applications.

VII. CONCLUSION

This project presented an energy-efficient sequential circuit design using an optimized clock-gated Johnson counter for low-power VLSI applications. In conventional sequential circuits, continuous clock switching leads to unnecessary dynamic power dissipation even when the circuit is not performing meaningful operations. To overcome this issue, the proposed design incorporates a clock-gating technique that selectively enables the clock signal only during required state transitions.The Johnson counter architecture was designed using Verilog HDL and verified through RTL simulation to ensure correct functional behavior. After simulation, the design was synthesized and analyzed to evaluate power consumption and performance. The results demonstrate that the optimized clock-gated Johnson counter effectively reduces dynamic power consumption by minimizing redundant clock switching activity while maintaining correct counter functionality.For practical validation, the design was implemented on an Altera Cyclone II FPGA development board using the Quartus Altera design software**.**The hardware implementation successfully demonstrated the working of the Johnson counter, where the output states were verified through LED indications. The synthesis and power analysis results obtained from the Quartus tool confirmed the reduction in switching activity and improved power efficiency compared to conventional counter designs.Overall, the optimized clock-gated Johnson counter provides a simple, reliable, and power-efficient solution for sequential circuit design. The combination of clock-gating techniques, Verilog HDL design, and FPGA implementation using Quartus ensures that the proposed system is practical and scalable for real-world applications. Therefore, this approach is well suited for integration in modern low-power VLSI systems such as embedded devices, portable electronics, and battery-operated applications.Future work may focus on implementing advanced clock-gating strategies and integrating additional power optimization techniques such as voltage scaling and adaptive power management to further improve energy efficiency in next-generation digital systems.

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